

## 100V N-Ch Power MOSFET

### Feature

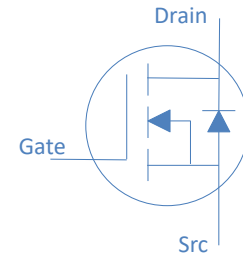
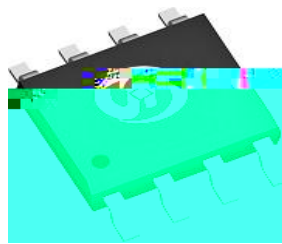
- High Speed Power Switching, Logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

$V_{DS}$		100	V
$R_{DS(on),typ}$	$V_{GS}=10V$	7	m
$R_{DS(on),typ}$	$V_{GS}=4.5V$	9.0	m
$I_D$		14.4	A

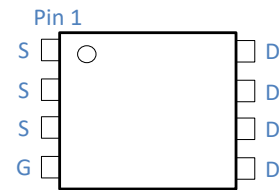
### Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

SOIC-8



Part Number	Package	Marking
HGS080N10AL	SOIC-8	GS080N10AL



Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C$	14	A
		$T_C$	9	
Drain to Source Voltage	$V_{DS}$	-	100	V
Gate to Source Voltage	$V_{GS}$	-	20	V
Pulsed Drain Current	$I_{DM}$	-	160	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.4mH, T_C$	245	mJ
Power Dissipation	$P_D$	$T_C$	3.1	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Lead	$R_{JL}$	25	
Thermal Resistance Junction-Ambient (steady state)	$R_{JA}$	40	
		75	

**Electrical Characteristics at T<sub>j</sub>      !      a      b      bb      "**
**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\text{ A}$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\text{ A}$	1.4	1.7	2.4	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=100V, T_j$	-	-	1	A
		$V_{GS}=0V, V_{DS}=100V, T_j$	-	-	100	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} \quad \quad \quad V_{DS}=0V$	-	-	100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	7	8	m
		$V_{GS}=4.5V, I_D=10A$	-	9	10.5	
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$	-	60	-	S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}\text{ Open}, f=1\text{MHz}$	-	1.3	-	

**Dynamic Characteristics**

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$	-	1876	-	pF
Output Capacitance	$C_{oss}$		-	348	-	
Reverse Transfer Capacitance	$C_{rss}$		-	5.6	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=50V, I_D=20A, V_{GS}=10V$	-	32	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	16	-	
Gate to Source Charge	$Q_{gs}$		-	6	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	4	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=10\text{ }\Omega$	-	7	-	ns
Rise time	$t_r$		-	4	-	
Turn off Delay Time	$t_{d(off)}$		-	20	-	
Fall Time	$t_f$		-	3	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R=50V, I_F=20A, dI_F/dt=500A/s$	-	40	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	160	-	nC

Fig 1. Typical Output Characteristics

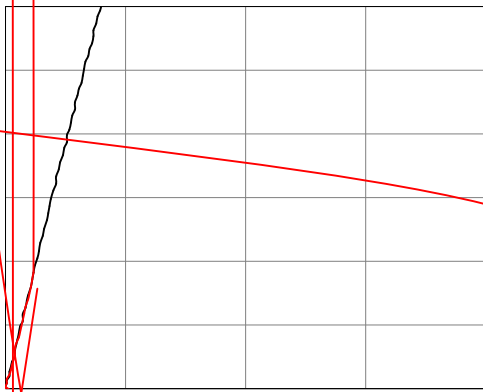


Figure 2. On-Resistance vs. Gate-Source Voltage

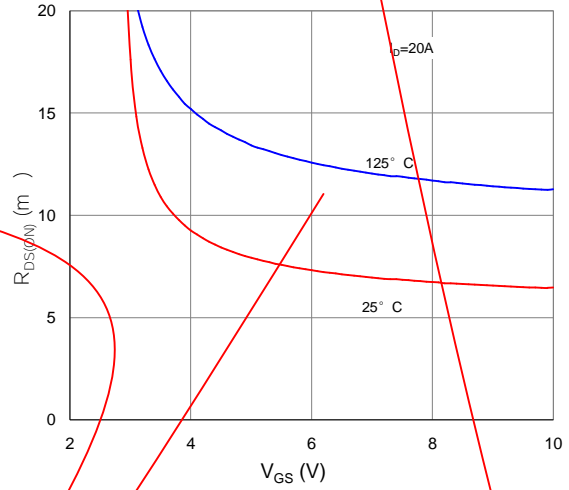


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

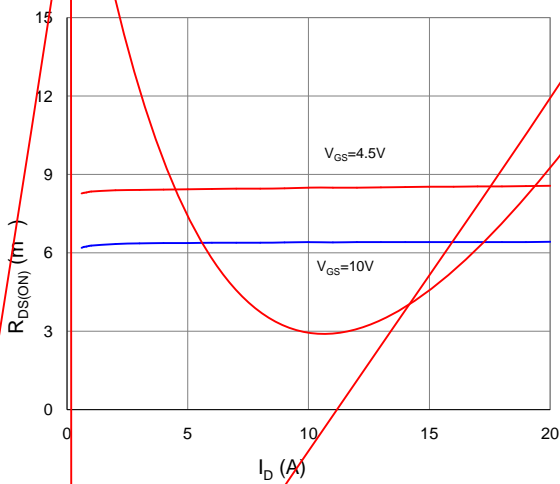


Figure 4. Normalized On-Resistance vs. Junction Temperature

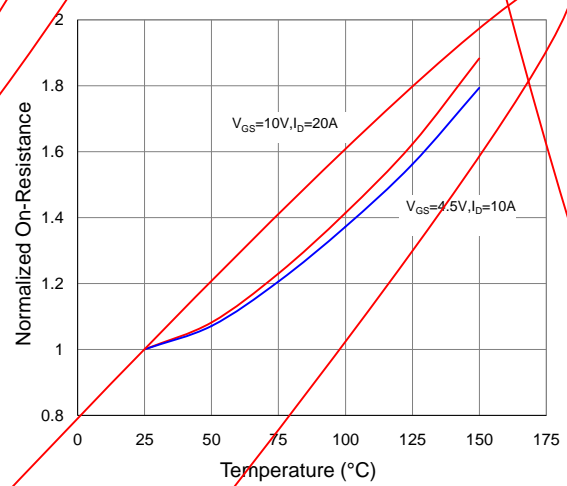


Figure 5. Typical Transfer Characteristics

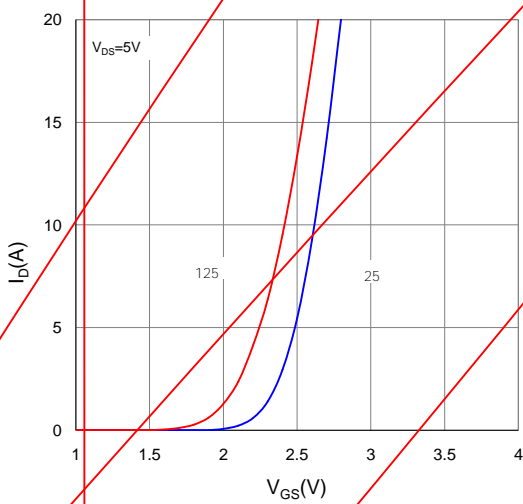


Figure 6. Typical Source-Drain Diode Forward Voltage

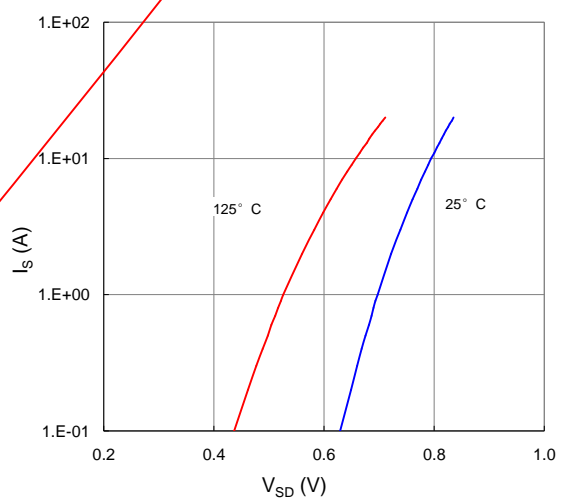


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

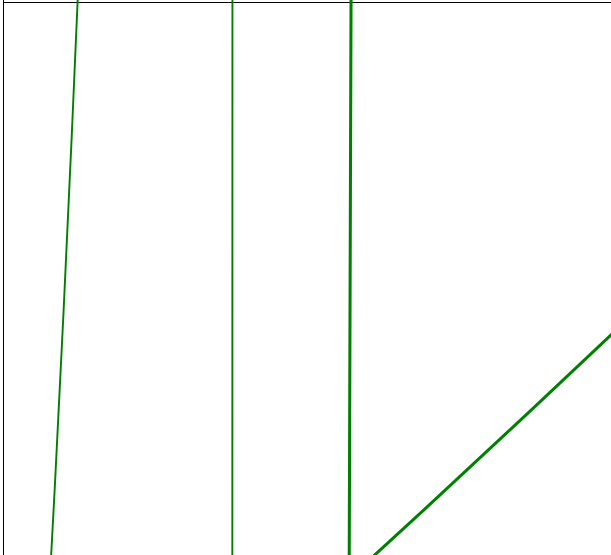


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

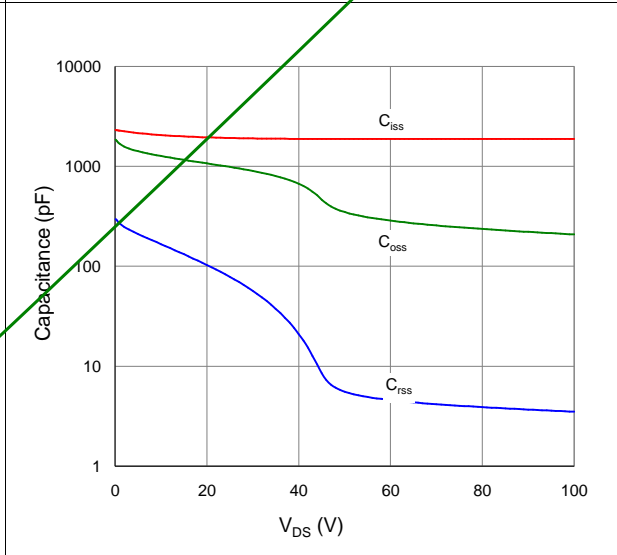


Figure 9. Maximum Safe Operating Area

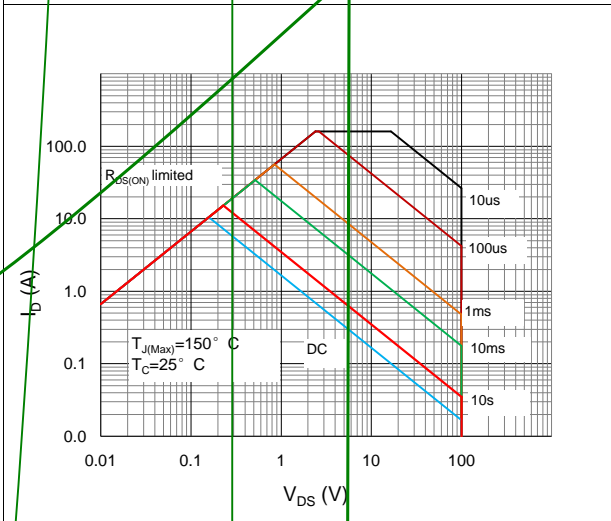


Figure 10. Maximum Drain Current vs. Case Temperature

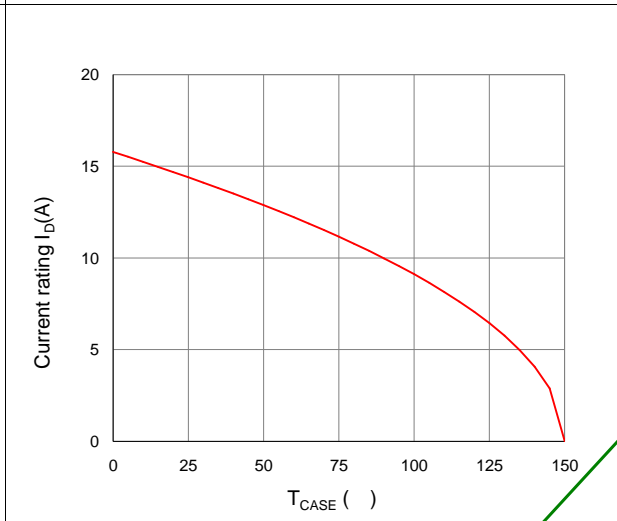
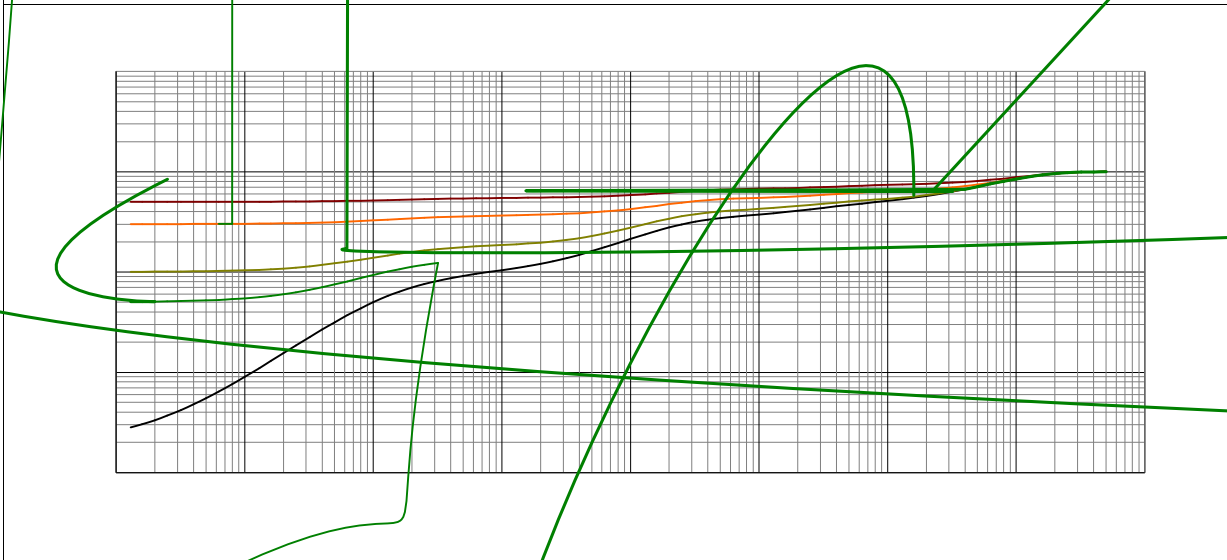


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



## Inductive switching Test

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## Gate Charge Test

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## Uclamped Inductive Switching (UIS) Test

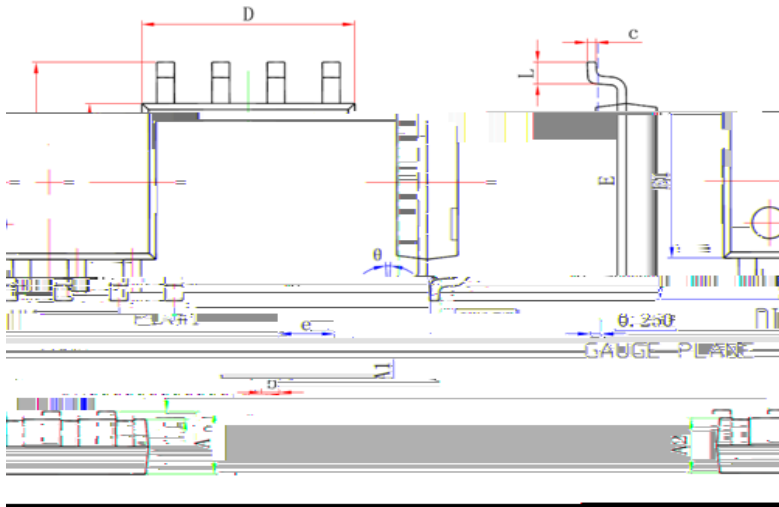
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## Diode Recovery Test

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Package Outline

SOIC-8, 8 leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (SBC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.031
theta	0°	8°	0°	8°